METHOD OF FORMING A CONTACT IN A SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a method of fabricating a semiconductor device, and more particularly, to a self-aligned contact method of forming a contact for a source/drain region of the semiconductor device.

[0002] A claim of priority is made to Korean Patent Application No. 2002-73049, filed on 22 November 2002, which is incorporated herein in its entirety by reference.

2. Description of the Related Art

[0003] As semiconductor devices become highly integrated, the distance between device components decreases, making it difficult to employ conventional patterning techniques. For example, when a contact is formed in an active region of a dynamic random access memory (DRAM) device, a contact area is so small that many problems are encountered during patterning of layers of the device. As such, a technique known as self-aligned contact formation has been introduced in an effort to combat the problems associated with the patterning of extremely small dimensions.

[0004] FIGS. 1 and 2 are cross-sectional diagrams for explaining a conventional self-aligned contact formation process. Referring first to FIG. 1, an isolation insulating film 1110 is formed in a semiconductor substrate 100 to define a device formation region. A gate dielectric film (not shown), gate conductive films 1123 and 1125, and a mask insulating film 1127 are formed in the device formation region, and an insulating film spacer 1129 is formed at the sidewalls of the gate conductive films 1123 and 1125 and the mask insulating film 1127 to define a gate 1120. A source region 1105a and a drain region 1105b are formed at respective sides of the gate 1120. After an etch stop 1140 is formed, a first interlayer insulating film 1150 is formed on the etch stop 1140, and a self-aligned contact hole 1160a is formed in the first interlayer insulating film 1150 through a predetermined patterning process.

[0005] Referring to FIG. 2, the etch stop 1140 remaining in the self-aligned contact hole 1160a is removed by dry etching, thereby exposing the source region 1105a and the drain region 1105b. The contact hole 1160a is filled with conductive polysilicon (not shown) to form a contact pad.

[0006] In the conventional self-aligned contact formation process, over etching of the etch stop 1140 remaining in the contact hole 1160a is needed to sufficiently expose the underlying surface of the silicon substrate 100. Unfortunately, due to characteristics of dry etching, the over etching can damage the silicon substrate 100, which in turn can increase the contact resistance of the contact hole 1160a. The result can be contact failures and increased leakage current.

SUMMARY OF THE INVENTION

[0007] According to one aspect of the present invention, there is provided a method for fabricating a semiconductor device in which a gate is formed on a device formation region of the semiconductor substrate, and source and drain regions are formed in the device formation region of the semiconductor substrate adjacent respective sides of the gate. The gate is formed to include a gate dielectric layer, a gate conductive layer and sidewall spacers located at respective sidewalls of the gate conductive layer. An etch stop layer is formed over the source region, the drain region and the sidewall spacers of the gate to obtain an intermediate structure, and a planarized first interlayer insulating film is formed over a surface of the intermediate structure. The first insulating layer is dry etched until the etch stop layer over the source region, the drain region and the sidewall spacers is exposed to form self-aligned contact holes in the first interlayer insulating over the source region and the drain region, respectively. The etch stop layer is then wet etched to remove the etch stop layer over the source region, the drain region and the sidewall spacers, and respective contact pads are formed by filling the self-aligned contact holes with conductive polysilicon.

[0008] According to the invention, the etch stop layer is removed by wet etching when the contact holes are formed, to thereby avoid damage to the

source and the drain regions and the formation of defects in the surface of the semiconductor substrate. Thus, electric characteristics such as leakage current and contact resistance can be improved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The above objects and advantages of the present invention will become readily apparent form the detailed description that follows, with reference to the accompanying drawings, in which:

[0010] FIGS. 1 and 2 are sectional views for explaining a conventional self-aligned contact formation method used in the fabrication of a semiconductor device;

[0011] FIGS. 3 through 7 are sectional views for explaining a self-aligned contact formation method used in the fabrication of a semiconductor device according to the present invention; and

[0012] FIG. 8 is a flowchart showing processes of the self-aligned contact formation method according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0013] The present invention now will be described more fully with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete and will fully convey the concept of the invention to those skilled in the art.

[0014] FIGS. 3 through 7 are sectional views for explaining sequential processes of a method of fabricating a semiconductor device according to the present invention.

[0015] Referring to FIG. 3, an isolation insulating film 110 is formed in a semiconductor substrate 100 by using known device isolation technology to define a device formation region. A gate dielectric film 121 is formed in the device formation region, and gate conductive films 123 and 125 and a mask

insulating film 127 are sequentially formed on the gate dielectric film 121. In this embodiment, the gate dielectric film 121 is either a silicon oxide film or a silicon nitride oxide film SiON. The gate conductive films 123 and 125 are formed by combining conductive polysilicon with metal silicide. In addition, the mask insulating film 127 is a silicon nitride film formed by chemical vapor deposition (CVD).

[0016] A photoresist (not shown) is formed in the mask insulating film 127, and a gate pattern is formed in the photoresist by using known alignment exposure processes. The mask insulating film 127 is etched to form a hard mask 127 by dry etching in which the patterned photoresist is used as a mask. After the photoresist mask is removed, the gate pattern is transferred to the gate conductive films 123 and 125 using the hard mask 127 as an etching mask. Then, a gate 120 is formed by forming an insulating film spacer 129 made of a silicon nitride film at the sidewalls of the hard mask 127 and the gate conductive films 123 and 125. Hereinafter, the hard mask 127 is denoted by the same reference numeral as the mask insulating film.

[0017] A source region 105a and a drain region 105b are formed on the semiconductor substrate 100 at both sides of the gate 120 by ion implantation in which the gate 120 is used as a mask. Here, a lower oxide film (not shown) may be formed in the source region 105a and the drain region 105b of the device formation region. The lower oxide film may be formed by thermal oxidation or may be the gate dielectric film 121 remaining in the device formation region.

[0018] A buffer layer 130 and an etch stop layer 140 are sequentially formed on the whole surface of the semiconductor substrate 100. The buffer layer 130 serves as a stress buffering layer between the etch stop 140 and the semiconductor substrate 100 in order to prevent stress from being applied to the semiconductor substrate 100 when the etch stop 140 is formed. If an oxide film remains on the source region 105a and the drain region 105b, it may not be necessary to form the buffer layer 130. The buffer layer 130 is a silicon oxide layer formed by chemical vapor deposition (CVD). In particular, it is desirable that the buffer layer 130 be a mid-temperature oxide (MTO) film that

is formed by low pressure chemical vapor deposition and is deposited at a temperature of 500℃ through 600℃. This is because the buffer layer 130 can exhibit a high etch rate and a high etching selectivity in an etch solution, i.e., ammonium hydroxide (NH4OH) solution. The etch stop 140 is a silicon nitride film formed by chemical vapor deposition (CVD) and has a high etching selectivity to the first interlayer insulating film 150 as the silicon oxide film. Thus, the etch stop 140 is effectively used when the contact hole is formed.

[0019] Still referring to FIG. 3, a first interlayer insulating film 150 is thickly formed on the whole surface of the semiconductor substrate 100, and its surface is planarized by a known planarization process. If the hard mask 127a and the insulating film spacer 129 are nitride films in order to perform a self-aligned contact formation process, it is desirable that the first interlayer insulating film 150 be a silicon oxide film formed by chemical vapor deposition (CVD) so that the first interlayer insulating film 150 can have a high etching selectivity with respect to the hard mask 127 and the insulating film spacer 129 as the silicon nitride films. In particular, it is desirable that the first interlayer insulating film 150 be a silicon oxide film formed by high-density plasma chemical vapor deposition (HDP CVD) because the deposition is executed rapidly, and the capability to fill the pattern is superior. When the etch stop 140 and the buffer layer 130 are removed by wet etching, the first interlayer insulating film 150 formed by HDP CVD is etched much slower than the etch stop 140 and the buffer layer 130 by an etchant solution. Thus, damage to a contact pattern by wet etching can be reduced.

[0020] The first interlayer insulating film 150 can be planarized by dry etching-back or chemical mechanical polishing (CMP). However, it is desirable that chemical mechanical polishing be used because it causes less damage to the semiconductor substrate 100.

[0021] After the planarization process is completed, it is desirable that the remaining thickness of the first interlayer insulating film 150 be higher than a predetermined height from an upper portion of the gate 120, thereby easily forming a self-aligned contact hole 160a of FIG. 6 when self-aligned contact hole etching is performed.

[0022] Referring to FIG. 4, the first interlayer insulating film 150 that is planarized is covered with a photoresist (not shown), and a self-aligned contact pattern is formed on the photoresist by alignment exposure. Here, the self-aligned contact pattern is formed to connect the source region 105a with the drain region 105b. The self-aligned contact hole 160a is formed by etching the first interlayer insulating film 150 by dry etching in which the patterned photoresist is used as a mask. Here, an upper portion of the etch stop 140 serves as an etching stopping boundary, and thus etching of the self-aligned contact hole 160a is stopped on the etch stop 140. Then, the insulating film spacer 129 partially serves as a mask, and thus the self-aligned contact hole 160a is formed at sides of the insulating film spacer 129.

[0023] FIGS. 5 and 6 will be described with reference to the flowchart of FIG. 8.

[0024] Referring to FIGS. 5 through 8, the etch stop 140 is removed by wet etching to expose the buffer layer 130. An upper portion of the etch stop 140 is cleaned by removing many residual products and polymers remaining on the semiconductor substrate 100 by using diluted hydrofluoric acid (HF) solution (step S1). Then, the silicon nitride film etch stop 140 is removed using an etching solution including phosphoric acid H_3PO_4 (step S2). Here, it is desirable that the etching solution including phosphoric acid H_3PO_4 be at a temperature of 120℃ to 150℃ to improve etching conditions, and have a density of 50wt% to 85wt% to obtain an appropriate etching rate. In general, the etching rate of the silicon oxide film (e.g., HDP silicon oxide film, HTO and MTO, or the like constituting the first interlayer insulating film 150) in the etching solution including phosphoric acid H_3PO_4 is 1Å through 4Å per minute.

[0025] Referring to FIGS. 6 through 8, the buffer layer 130 is removed by wet etching to expose the semiconductor substrate 100 of the source region 105a and the drain region 105b (step S3). Here, an etching solution is used to etch the silicon oxide film buffer layer and is an ammonium hydroxide (NH_4OH) solution at a temperature of 30℃ to 80℃. Thus, an etching rate of the silicon oxide film increases, and the time required by the entire process can be greatly reduced. While an etching process is in progress, the first interlayer insulating

film 150, which is a silicon oxide film formed by HDP CVD, is also etched. However, an etching rate of the first interlayer insulating film 150 is about 2Å per minute. Since the etching rate of the first interlayer insulating film 150 is slower than that of the buffer layer 130 as the etching rates of a mid-temperature oxide (MTO) film, the buffer layers 130, and the first interlayer insulating film 150 are about 5Å and hundreds of Å respectively while thousands of Å of the first interlayer insulating film 150 is etched per minute. Therefore, this wet etching hardly causes damage the contact hole morphology considering changes in sizes of the contact hole.

[0026] The etching solution should have a high etching rate with respect to the buffer layer 130 and a low etching rate with respect to the first interlayer insulating film 150. Thus, the etching solution is formed by combining ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2), and deionized water. In particular, the etching solution of the oxide film should include 0.1 wt% through 1.0 wt% of ammonium hydroxide, and 4.0 wt% through 7.0 wt% of hydrogen peroxide. Thus, when the buffer layer 130 is etched, the first interlayer insulating film 150 can firmly maintain the self-aligned contact hole 160a. The etching solution including ammonium hydroxide (NH_4OH) does not causes damage to the silicon substrate of the semiconductor substrate 100, and thus the source region 105a and the drain region 105b can be exposed without causing any defects or stress.

[0027] Referring to FIG. 7, sufficient conductive polysilicon is formed on the whole surface of the semiconductor substrate 100 to fully fill the self-aligned contact hole 160a. Then, the conductive polysilicon is removed by chemical mechanical polishing it until it reaches the level of the upper portion of the first interlayer insulating film 150. Then, the self-aligned contact hole 160a is filled with the conductive polysilicon, and thus a contact fill or a contact pad 160 is formed.

[0028] As described above, the method for fabricating a semiconductor device according to the present invention removes the etch stop 140 and the buffer layer 130 by wet etching when the contact hole is formed, and thus an additional cleaning process is not needed.

[0029] That is, when the contact hole is formed according to the conventional method, the etch stop 140 is removed by wet etching to expose the semiconductor substrate 100, and then is further cleaned to remove polymers or residual particles due to wet etching. Thus, the time required for forming the contact hole is increased.

[0030] However, in the present invention, the etch stop 140 and the buffer layer 130 are etched by wet etching. In particular, the ammonium hydroxide (NH_4OH) solution, which is used to etch the buffer layer 130, also serves as a cleaning solution, and thus an additional cleaning process is not needed. As a result, the time required for forming the contact hole is reduced to about half that required for the conventional method.

[0031] According to the present invention, the etch stop layer at the bottom of the contact hole is removed by wet etching when the contact pads connecting the source region with the drain region are formed, to thereby avoid damage to the source and the drain regions and the formation of defects in the surface of the semiconductor substrate. Thus, electric characteristics such as leakage current and contact resistance can be improved.

[0032] While this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.